

## BittWare, FçFÔ FPGA G0G=GIGwGzGŠGEGuG•G6GQGF GCGŠG^ TeraBox 200DE G"ŠÎ/2

(•\GYGsGŠG]G•GeGEGqGŠ ^GAG•200DE v 15  
 ¥ - G6G•GMGŠGeGwG2GHPGAGCGGFGIGwGzGŠGI  
 FpGxGŠGUG1G•G>GCGeGwG200DEŠFpBittWare 4Š  
 6ÚFÿF, G FôFiFß, FçFÔG6GQGF GCGŠG^200DEFA  
 G"ŠÎ/2FçG FçFiTeraBox 200DE FÿF, GUGŠGMIG•GMK  
 GCGŠG^TeraBox G"GgGŠGGFû S( FâG FöFÚG F, G6GQGF G0Ge  
 GxG?GŠGEGuG•Fû0[ ÓFâG G G G T7'F÷4#4Fâ#ÚGFGwG6FPGA G0G=GIGwGzGŠGEGuG•G" Ž6äFéG Fä  
 FøFÜ •+ F÷Fé200DE FÿF, ,FçFÔ DELL PowerEdge™ XE2420 G"GgGŠGGF, 0¿\*(8' Fp`FâFÔ2U  
 GCGŠG^GŠF÷FéF'9x ØFû S6Ú iFâGFFVF, £ ( ÒF, µ" Ú\*f N1=FúFûFpG)GŠG=G{GŠGW FôFö  
 G FéG Fé0 7§ iFéG 0[ óFû P ÂFéG FiGAchronixFIntelFXilinx Fp q, FPGA G"i©FøFéG œ ÈFÔ  
 BittWare G0G=GIGwGzGŠGM0 G" /æF÷FÝG FéF'



BittWare FpGIGŠG?GTG1G•G> , \j&k6xF÷FôG Petrie FÿF, FpG FÖFû3ÚG FöFÔG GCGŠG^GCGeGw  
 G2GrGŠFÜ f jFéG G6G•GMGŠGeGwG2GHPGAGCGGFGCGŠG^GŠGeGwGQGVGcG7GŠGnFÜ Y2ŠFçFöFÔG FiG  
 FÜ9x ö+FúFPGA GgGŠGGFpGKGxGsGŠGEGuG•G"G6GQGF Fú4Ä FéG Fÿ T7'F÷FçFiF'GCG2GHF, 5 5 F, 7Á Š  
 óFÿF, 5 0[Fú1"8ÿF÷FéF'FÚ ]Fÿ3û -F, "+-FpG9GGGMnGeGwGQGVGcG7GŠGnG"0¿FçGK, G FçFßFÿF'  
 GŠGVFÚG G ö ?FúGwG2GcGCG2G=Gy'ö#.Fû P ÂFçFöFÔG GCGeGwG2GrGŠFø ŠFéBittWareFÜ FòG G FçFiF  
 FÿF Dell OEM Fø6x ° ŠFçFöF, PowerEdge XE2420 FûFôFÔFö ÚG F, a æFp FPGA G0G=GIGwGzGŠGMG"  
 1 FéG µ G" "G FçFi F'FâFpŠFÚG G F, 4#4Fú#" FÚG 0 7§F÷0£'i7ÿ(Ù °FpG)GŠG=G{GŠGW ¥FâFú0¿  
 0£FâG FiF, q 6FpG6G•GMGŠGeGwG2GHPGAGCGGFGCGŠG^GŠTeraBox 200DE FÜ#ÔG G G Fç  
 FiF'FÄ

### 200DE

BittWare FpTeraBox 1 GCGŠG^GŠGeGwGQGVGcG7GŠGn0 \*LFPGA, F0G=GIGwGzGŠGMG" FøFöFÚG F,  
 GxGGG=FøGAGGGVG" P öFçFúFÜG F, 6ä\$IFø Ž6äG"3200DE-FÿçFâF+ Fÿ FpFøFÚG F÷FéF'  
 x %-FÔ ß/œFÝZp GwGQG=GCGŠG^GŠ  
 x 2 FôFp" 2 a æ Intel® Xeon® GGG?GŠGdGyGeG{GIGQGC  
 x G[GQGVG]GŠG= µ p S( GEGNBSCHG:G2GWG FÜGZGF0è9, í

- x Ć G · 8 ØH 5°CHZ40CH
- x G8GeGEGuG•FpGcG1GyGMGŠ ŪFÝGgGJGyF÷ ; ÖFÛG -1¼
- x GoG•GTGXG•GGFÛ ÆFúGcG{G•G700SŠG•G•GWG0GŠG}aGG ö
- x 2 FôFpFHFL PCIe G0G=GIGwGzGŠGMG9GŠGWFPgCGkGŠGV
- x AchronixF]Intel G FiFyXilinx FPGA G"š3UFçFiFPGA G0G=GIGwGzGŠGMFp4E ¥
  - o [S7t-VG6](#) FyF]Achronix Speedster7t FPGA FÚG G400GbE G[GQGVG}GŠG" š3U
  - o [520N-MX](#) FyF]Intel Stratix 10 MX Fø16GB HBM2 GoGpGxG" š3U
  - o [XUP-P3R](#) FyF]Xilinx UltraScale+ FPGAF,9x ØFúG=G{GQG= ‡FÚG G GVGxG:GŠ µ+ G" Fø4 FôFp100GbE G[GQGVG}GŠG" š3U
- x BittWare FpM.2FU.2FEDSFF 0 G" Q#ÝFçFi3ã •Fp FPGA Ć G µ+
- x GCGŠG^GŠFPA G]GŠGWG4G5G0G"G9G^GŠFéG 160\$•FÛ
- x BittWare G FiFyDELL Technologies FÚG %\$ K @ e •+

BittWare TeraBox Fp#. ÖF, w · ¥F, G?GŠGGGGMGUG1F, z Š0 G"0ò3ÙFéG ,FçFÔG4G5GaGXGŠFy  
[www.BittWare.com](http://www.BittWare.com) F÷Fä0tFÔFiFöFáG FéF¹

**BittWare FÚFôFÔFö**

GpGzGQG=GGFpG>GyGŠGe BittWare FyFAG•GbGsGŠGVF, G[GQGVG}GŠG=F, GGGVGzGŠGFF, GIG•GCG  
 G> ¥Fä ÷ AchronixF]IntelF]Xilinx FPGA GTG=G\GŠG" I ©FøFéG G6G•GMGŠGeGwG2GHG=GwGGFpG0G=GIGwG  
 0 G" f jFçFöFÔG FéF¹FäG G FpGeG{G>GwGIGdGYOÖE" P öFéG Fø iFúG6G[GyG<GŠ FäG0GeGx  
 G?GŠGEGuGŠGx Fú ¥ VFçG FéF¹BittWare Fy 30 °FúG FiFóFôFPGA G0G=GIGwGzGŠGMFp6ã\$!) 9,FÛFÖ  
 G F,5 #0÷ FPGA G0G=GIGwGzGŠGMG" Ž6äFéG FÚ ]Fú PFçFöG6G•GMGŠGeGwG2GHG=GwGGFp1 F, è  
 GCG2GFçGCGkGŠGV0[ óFú P ÁFéG FäFøFÛPFAVCGG•GNŠK ĆFçFúFÔ MF]GCGeGwG2GrGŠF÷Fé  
<http://www.bittware.com>

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**GpGzGQG=GGFôFôFôFö**

GpGzGQG=GGFyF, • 1]Fp š8 FøG G 1IFÚFú#Ö qG" #FäFéG GTG=G\G{GFGŠG" •+ FúFéG FäFøF÷FôFúFÛG  
 -FøFöFÔFöF¹ #0 Gf \ è VF÷ | G" Ž6äFçF, GUGŠGM3û TMF, GŠG•GNGGVGxG0GyF, +- .34F, 7ÁFúFúFp  
 ]F»Fú w Fú È( Fú K)FGEGGTGnF, GCGŠGaGGFÚG G 7Á ÈGKGxGsGŠGE GúG•G" f jFçFöFÔG  
[www.japanese.molex.com](http://www.japanese.molex.com)

**GpGzGQG=GGFp ›' GCG2GVFúFôFôFôH ,e1 H**

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